AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A switching regulator converting an input voltage into a predetermined constant voltage and outputting the constant voltage from an output terminal, the switching regulator comprising:

a switching transistor controlling output of the input voltage by switching in accordance with a control signal input to a control electrode;

a smoothing circuit part configured to smooth an output voltage of the switching transistor and output the smoothed output voltage to the output terminal;

a control circuit part configured to control the switching of the switching transistor in synchronization with an externally input clock signal so that a voltage at the output terminal is the predetermined constant voltage; and

a clock signal detector circuit part configured to detect presence or absence of inputting of the clock signal,

wherein upon detecting stoppage of the inputting of the clock signal, the clock signal detector circuit part causes the control circuit part to stop operating and perform a standby operation for reducing power consumption and thereby to turn off the switching transistor, and

wherein the switching transistor, the control circuit part, and the clock signal detector circuit part are integrated into a single IC.

2. (Original) The switching regulator as claimed in claim 1, wherein upon detecting the inputting of the clock signal, the clock signal detector circuit part causes the control circuit part to start operating and perform a normal operation and thereby to perform the switching of the switching transistor.

3. (Original) The switching regulator as claimed in claim 1, wherein the clock signal detector circuit part comprises:

an edge detector circuit configured to detect at least one of a rising edge and a falling edge of signal level of the clock signal and output a pulse of a predetermined pulse width for the detected at least one of the rising edge and the falling edge every time the at least one of the rising edge and the falling edge is detected;

an integrating circuit configured to charge a capacitor with a preset time constant;

a switching device configured to release an electric charge stored in the capacitor upon the outputting of the pulse from the edge detector circuit; and

a binarizing circuit configured to generate a control signal to perform operation control of the control circuit part by converting a terminal voltage of the capacitor into a binary signal, and output the generated control signal.

4. (Original) The switching regulator as claimed in claim 3, wherein the time constant is preset for the integrating circuit so that a period between stoppage of the release of the electric charge stored in the capacitor by the switching device and completion of the charging of the capacitor up to a predetermined voltage is longer than an interval at which the pulse is output from the edge detector circuit.

5. (Original) The switching regulator as claimed in claim 1, wherein the control circuit part comprises:

a reference voltage generator circuit configured to generate and output a predetermined reference voltage;

an output voltage detector circuit configured to detect the voltage at the output terminal, and generate and output a voltage proportional to the detected voltage;

an error amplifier circuit configured to compare the reference voltage and the proportional voltage, amplify a voltage difference between the reference voltage and the proportional voltage, and output the amplified voltage difference as an output voltage;

a triangle wave generator circuit configured to generate and output a predetermined-triangle wave signal synchronizing with the clock signal;

a PWM circuit configured to compare the output voltage of the error amplifier circuit and voltage of the triangle wave signal output from the triangle wave generator circuit, and generate and output a pulse signal for performing PWM control, the pulse signal having a pulse width according to the output voltage of the error amplifier circuit; and

a drive circuit configured to control the switching of the switching transistor in accordance with the pulse signal from the PWM circuit,

wherein upon the stoppage of the inputting of the clock signal, the clock signal detector circuit part causes each of the error amplifier circuit, the triangle wave generator circuit, the PWM circuit, and the drive circuit to stop operating and perform the standby operation for reducing power consumption and thereby to turn off the switching transistor.

6. (Original) The switching regulator as claimed in claim 5, wherein the clock signal detector circuit part determines that the inputting of the clock signal is stopped if a frequency of the triangle wave signal output from the triangle wave generator circuit does not fall within a predetermined range.

7. (Original) The switching regulator as claimed in claim 6, wherein the clock signal detector circuit part detects presence or absence of inputting of the clock signal to the triangle wave generator circuit, and causes the control circuit part to start operating and perform a normal operation and thereby to perform the switching of the switching transistor upon detecting the inputting of the clock signal to the triangle wave generator circuit after determining that the inputting of the clock signal is stopped.

8. (Original) The switching regulator as claimed in claim 5, wherein the triangle wave generator circuit comprises:

a PLL circuit, the PLL circuit including:

a waveform shaping circuit configured to convert the triangle wave signal into a rectangular wave signal by shaping the triangle wave signal, and output the rectangular wave signal;

a phase comparator configured to compare phases of the clock signal and the output signal of the waveform shaping circuit, and output a voltage according to a result of the comparison;

a filter circuit configured to smooth the output voltage of the phase comparator and output the smoothed voltage; and

a triangle wave oscillator configured to generate and output the triangle wave signal of a frequency according to the output voltage of the filter circuit,

wherein upon the stoppage of the inputting of the clock signal, the clock signal detector circuit part causes each of the waveform shaping circuit, the phase comparator, and the triangle wave oscillator to stop operating.

9. (Original) The switching regulator as claimed in claim 1, wherein the smoothing circuit part comprises a transistor for synchronous rectification connected in series to the switching transistor;

the control circuit part controls switching of the transistor for synchronous rectification; and

the switching transistor, the transistor for synchronous rectification, the control circuit part, and the clock signal detector circuit part are integrated into a single IC.

10. (Original) The switching regulator as claimed in claim 9, wherein the IC comprises:

a first power supply terminal to which positive supply voltage is applied, the positive supply voltage forming the input voltage to be converted into the predetermined constant voltage;

a second power supply terminal to which negative supply voltage is applied;

a pulse output terminal from which a pulse signal from the switching transistor is output;

an output voltage input terminal to which the voltage output from the output terminal is input; and

a clock signal input terminal to which the clock signal is input.

11. (Canceled)

12. (Currently Amended) The switching regulator as claimed in claim [[11]] 1, wherein the IC comprises:

a first power supply terminal to which positive supply voltage is applied, the positive supply voltage forming the input voltage to be converted into the predetermined constant voltage;

a second power supply terminal to which negative supply voltage is applied;

a pulse output terminal from which a pulse signal from the switching transistor is output;

an output voltage input terminal to which the voltage output from the output terminal is input; and

a clock signal input terminal to which the clock signal is input.

13. (New) A method for operating a switching regulator, the method comprising:

detecting a clock signal;

grounding a determination node when the clock signal rises;

allowing the potential at the determination node to rise above a threshold level if the clock signal does not rise;

asserting a standby signal if the potential at the determination node rises above the threshold level; and

causing a control circuit to stop operating when the standby signal is asserted.

14. (New) A method for placing a switching regulator in a standby state, the method comprising:

detecting a clock signal;

grounding the potential at a determination node when the clock signal rises;

allowing the potential at the determination node to rise above a threshold level if the clock signal does not rise; and

asserting a standby signal if the potential at the determination node rises above the threshold level.

15. (New) The method of claim 14, wherein the step of grounding the potential at a determination node further comprises:

inverting the clock signal to create an inverted clock signal;

comparing the clock signal to the inverted clock signal to determine a period of delay caused by said inverting to create a comparison voltage; and

activating the gate of a transistor with the comparison voltage when the comparison voltage is high to ground the potential at the determination node.

16. (New) The method of claim 14, wherein the steps of allowing the potential at the determination node to rise further comprises:

inverting the clock signal to create an inverted clock signal;

comparing the clock signal to the inverted clock signal to determine a period of delay caused by said inverting to create a comparison voltage; and

deactivating the gate of a transistor with the comparison voltage when the comparison voltage is low to allow the potential at the determination node to rise.